REJECTIONS UNDER 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin *et al.* ("On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter," IEEE Transactions on Electron Devices, Vol. 45, No. 8, August 1998, hereinafter "Jin") in view of Ishibashi et al. (USP 6,864,539, hereafter "Ishibashi") and further in view of Shimomura et al. (JP 10-189957, hereafter "Shimomura"). This rejection is respectfully traversed.

Claim 1 recites a lateral bipolar CMOS integrated circuit wherein, [an] n-channel MOS transistor **operates** in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an **operation mode** of an npn lateral bipolar transistor which is inherent in the n-channel MOS transistor, and [a] p-channel MOS transistor **operates** in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an **operation mode** of a pnp lateral bipolar transistor which is inherent in the p-channel MOS transistor. (Emphases Added)

It is alleged in the Office Action at page 3 that the inverter chain of FIG. 3 of Jin teaches the structure of the n-channel and p-channel MOS transistor as recited in claim 1 and the inverter chain will therefore inherently function in a hybrid mode.

However, the Dynamic Threshold SOI CMOS Inverter (DTMOS) of FIG. 3 of Jin does not include an npn or a pnp transistor inherently. As illustrated in FIG. 3, there are six (6) MOS transistors and each MOS transistor includes two (2) diodes (Dn1 and Dn 2, for example), and not npn or pnp transistors.

Additionally, the last paragraph (II. Power Dissipation Model for DTMOS Inverter) on page 1 of Jin discloses:

> The FIG. 3 shows the schematic of a DTMOS inverter chain. The <u>parasitic lateral bipolar inherent in the DTMOS will not turn on</u> in the inverter circuit as it is not biased in the forward active mode, so in the

> following analysis only the two back-to-back parasitic diodes behavior of DTMOS is considered.
>
> (Emphases Added)

Accordingly, the inverter chain of FIG. 3 of Jin will **not** inherently function in a hybrid mode.

As is illustrated in FIG. 1 of Jin, the DTMOS has a Source-Body (pn or np) junction and a Body-Drain (pn or np) junction. However, the distance between the source and drain may be large. Therefore, the Source-Body-Drain does not function as an npn or pnp transistor. Alternatively stated, the Source-Body-Drain does not function in transistor mode, even though the DTMOS may seem to have an npn or pnp structure.

As mentioned above, claim 1 requires "[an] n-channel MOS transistor **operates** in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an **operation mode** of an npn lateral bipolar transistor ... [a] p-channel MOS transistor **operates** in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an **operation mode** of a pnp lateral bipolar transistor. (Emphases Added)

Applicant submits that Jin discloses a DTMOS having pn and np junctions, however, for at least all the above reasons, these pn and np junctions do not operate as pnp transistor. Ishibashi and Shimomura fail to remedy the deficiencies of Jin. Therefore, the combination of Jin, Ishibashi and Shimomura, would fail to render the limitations of independent claim 1 obvious to one of ordinary skills in the art.

Applicant, therefore, respectfully requests that the rejection to claim 1 under 35 U.S.C. § 103 be withdrawn.

With regards to claims 2-8, Applicant respectfully asserts that claims 2-8 are dependent upon claim 1 and claim 1 has been shown patentable at least for the reasons set forth above. Therefore, claims 2-8 are patentable at least by reason of

their dependency. For at least this reason, Applicant respectfully requests that the rejections of claims 2-8 be withdrawn.

INTERVIEW REQUESTED

If the Examiner remains unconvinced by the arguments set forth above, the Examiner is respectfully requested to contact the undersigned at the number below to arrange for a mutually convenient time to conduct an interview in connection with the present application.

CONCLUSION

In view of the above remarks, Applicants respectfully submit that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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